Asynchronous Portfolio – Rajit Manohar Research Group

Architecture

Low-Power GPS Processor – D5548

An asynchronous GPS baseband processor architecture was devised that minimizes power consumption while providing continuous position information. The system achieves low power by allowing all subsystems to run at their natural frequencies without clocking and all signal processing is done on-the-fly. The technology decouples crucial GPS receiver operations from power-hungry post-processing. This allows the GPS receiver to be deployed anywhere to perform only crucial receiver operations and transmits just enough information back to the base station for further processing.

Publication: Tang, B.Z.; Longfield, S.; Bhave, S.A.; Manohar, R., "A Low Power Asynchronous GPS Baseband Processor," *18th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC),* May 2012

Energy-Efficient Pipeline Templates for High-Performance Asynchronous Circuits – D5479

Two energy-efficient pipeline templates for high-throughput asynchronous circuits were designed that greatly minimize handshake circuitry and power consumption by taking advantage of pre-existing timing assumptions. By reducing the handshake overhead and energy requirements for asynchronous quasi-delay-insensitive (QDI) circuits, the invention addresses a major constraint of QDI technology (desirable due to its robustness to process variations, lack of dependence on a global clock signal and inherent perfect clock gating), enabling it as a feasible alternative for future chip design.

Patent Application: WO2013020114

Publication: Sheikh, Basit and Manohar, Rajit, "Energy-Efficient Pipeline Templates for High-Performance Asynchronous Circuits," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Volume 7 Issue 4, Article 19, Dec. 2011

Zero-Delay Wakeup for Power-Gated Circuits – D5109

A new "zero-delay" latency hiding wakeup technique for power gated asynchronous circuits was developed at Cornell. The technology leverages the robustness of asynchronous circuits to delays and supply voltage variations, and can be used with any of the existing power gating schemes.

Patent Application: WO2011137339

Publications:

- Ortega, C.; Tse, J.; Manohar, R.; "Static Power Reduction Techniques for Asynchronous Circuits," *2010 IEEE Symposium on Asynchronous Circuits and Systems (ASYNC)*, May, 2010
- 5109 Technology Brief

Low-Power Double-Precision Floating-Point Adder and Multiplier – D5108

The first detailed design and implementation of an asynchronous, low-power, double-precision floating-point adder (FPA) and floating point multiplier (FPM) compliant with current standards are presented for vastly improved computing efficiency. Based on the energy consumption analysis of functional building blocks of a baseline FPA, the energy-efficiency was improved by exploiting data-dependent optimization techniques for each functional block. Circuit simulation of the baseline asynchronous FPA shows a throughput of 2.15 GHz while consuming 69.3 pJ per operation in a 65nm bulk process.

Patent Application: WO2011137209

Publications:

- Sheikh, B.R.; Manohar, R., "An Operand-Optimized Asynchronous IEEE 754 Double-Precision Floating-Point Adder," *2010 IEEE Symposium on Asynchronous Circuits and Systems (ASYNC).*
- Basit Riaz Sheikh and Rajit Manohar, "An Asynchronous Floating-Point Multiplier," *Proceedings of the 18th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, May 2012.
- 5108 Technology Brief

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Asynchronous Analog-to-Digital Converter – D3734
A novel asynchronous analog-to-digital converter (ADC) was developed that uses significantly less power than conventional ADCs. The new topology, referred to as "level-crossing flash-ADC (LCF-ADC), uses a non-uniform sampling technique by adopting an asynchronous event-driven circuit design and "level-crossing sampling". The LCF-ADC takes a sample only when the input signal crosses predefined voltage levels, thereby optimizing its sampling rate for current signal complexity. Unlike other asynchronous ADCs, the LCF-ADC uses a parallel topology and does not explicitly track the sampling time, allowing for additional power savings.
Patent: 7,466,258
Publication: Akopyan, F.; Manohar, R.; Apsel, A.B., "A level-crossing flash asynchronous analog-to-digital converter," *12th IEEE International Symposium on Asynchronous Circuits and Systems,* March 2006.

Processing Element Optimized for Event-Driven Applications – D3309
An event-driven processor architecture was developed and optimized for low energy requirements and data monitoring operations in sensor networks. The invention is event-driven with a low-overhead transition between active and idle periods, distinguishing it from a conventional microprocessor. Conventional processors have several sleep states whereas the invention's processor has a single sleep state, during which all switching activity stops. The time to wake up from this sleep state is merely tens of nanoseconds. Additionally, the processor includes a lower-power sleep mode and exhibits low power consumption when awake, providing the best of both worlds: the energy savings of "deep" sleep and the low wake-up latency of "light" sleep.
Patent: 7,788,332

Protocol

Self-timed Single-track Signaling Protocol – D5960
Single-Track Asynchronous Ternary Signaling (STATS) is a low energy, self-timed, single bit on-chip link to replace dual-rail encoding in wire-constrained situations, such as 3D inter-die communication using through-silicon vias (TSV). STATS combines all three wires in a traditional dual-rail encoding - true, false, and acknowledge - into a single wire. Five different self-timed single-bit on-chip links with widely varying properties were studied, including the new Cornell STATS link protocol. The analysis showed that STATS is a strong candidate for TSV due to its efficient use of resources. STATS yielded significantly higher energy-throughput and area-throughput per TSV than all other links. The technology can be extended to multiple bits in parallel over multiple wires.

Scalable Method for Discrete-Event Simulation on Parallel Machines – D3312
A new event synchronization protocol was created called time-based synchronization (TBS), suited for parallel discrete event simulation (PDES) of mobile ad hoc wireless networks. Unlike traditional protocols, there is no explicit communication to synchronize parallel processors, eliminating the bottleneck that limits the number of participating processors. The new protocol ultimately enables a fast simulation of wireless networks that runs many orders of magnitude faster than traditional methods. In particular, a Logical Process (LP) in a TBS-based simulation can determine whether an event is executable without waiting for information from other LPs. LPs in the network are independent of each other with an external comparison between timestamps for each event, and therefore, the simulation can be carried out at speeds faster than real time.
Patent: 7,564,809

Tools & Thermal Management

Automated Layout of Arbitrary Digital Circuits – D5921

A software tool was designed for automating the physical design of arbitrary digital asynchronous circuits, eliminating the need for mapping a digital circuit to a specific set of standard gates. This tool, called *CellTK*, generates customized logic that is compatible with currently available ASIC flows, enabling widespread adoption of asynchronous circuits to address increased process variation, susceptibility to environmental conditions, and other technology challenges facing chip designers. The CellTK mapping tool is able to produce layouts for any circuit, regardless of logic family and design paradigm, in a fraction of the design time required by hand-optimized custom designs.

Publication: Karmazin, R; Ortega Otero, C.T.; Manohar, R., "CellTK: Automated Layout for Asynchronous Circuits with Nonstandard Cells," *19th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC),* May 2013

Dynamic Thermal Management in Asynchronous Circuits – D3590

A novel scheme was devised to automatically regulate the performance and power consumption of asynchronous circuits with minimal implementation overhead, and without interruption of operation. The unique approach leverages the inherent temperature response of subthreshold transistors to construct simple temperature sensitive delay elements, which are strategically placed to regulate local throughput and modulate the circuit's temperature accordingly.

Patent: 7,411,436